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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,185	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 17-20* is/are rejected.

7)☒ Claim(s) *7,9,10,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed May 15, 2006 in response to the Office action dated November 23, 2005. Claims 13, 14, and 20 have been amended. Claims 1-20 are pending in this application.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's new declaration which was filed May 15, 2006 has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

OBJECTIONS

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The subject matter in question is disclosed in claim 1. The term "examining" in claim 1 does not appear anywhere in the detailed description of the preferred embodiments.

3. The new title of the invention is still not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "Dirty Cache Line Write Back Policy Based On Stack Size Trend Information."

4. In view of Applicant's amendment, the objections to the specification indicated in sections 6-11 of the Office action dated November 23, 2005 have been withdrawn.

Claims

5. In view of Applicant's amendment, the objections to **claims 12-15 and 20** have been withdrawn.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. **Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.** The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The subject matter in question is disclosed in claim 1. The term "examining" in claim 1 does not appear anywhere in the detailed description of the preferred embodiments. The Examiner is unclear as to the exact meaning of "examining" with regard to the patentability of claim 1.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-4, 8, 11, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Shen et al. (U.S. Patent 5,687,336).

10. **As per claim 1**, Shen discloses a method of managing memory, comprising:

examining current and future instructions operating on a stack (col. 3, line 65 – col. 4, line 7; col. 6, line 58 – col. 7, line 15; Figs. 2 and 4);

determining stack trend information (col. 4, lines 11-15 and 36-60; Fig. 2); *It should be noted that Shen's final value for the stack pointer indicates whether the stack size has increased or decreased.*

utilizing the trend information to reduce data traffic between various levels of a memory (col. 8, lines 34-47). *It should be noted that by having the stack pointer signal a mis-aligned access, push/pop pairing is prevented, a second cache access is prevented, thus, data traffic between various levels of the cache are reduced).*

11. **As per claim 2**, Shen discloses determining the trend information includes examining future instructions to determine if the size of the stack is going to decrease as a result of future instructions (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-5 and 9-10; Figs. 2 and 4).

12. **As per claim 3**, Shen discloses a predetermined number of instructions are used in determining stack trend information (col. 3, lines 65-67; col. 6, lines 47-48). *It should be noted that if there is only one instruction per stage and there are five stages in the pipeline, then five instructions are used in determining stack trend information.*

13. **As per claim 4**, Shen discloses the number of predetermined instructions is at least two (col. 3, lines 65-67; col. 6, lines 47-48). *See citation note for claim 3 above.*

14. **As per claim 8**, Shen discloses determining the trend information includes examining future instructions to determine if the size of the stack is going to increase as a result of future instructions (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-7; Figs. 2 and 4).

15. **As per claim 11**, Shen discloses a computer system, comprising:

a processor (col. 4, line 37; Fig. 2);

a memory coupled to the processor (col. 4, lines 33-34; Fig. 2, element 26); *It should be noted that the memory physically lies within the processor, thus making the memory and processor coupled.*

a stack that exists in memory and contains stack data (col. 4, lines 33-34; Fig. 2, element 26);

a memory controller coupled to the memory (col. 5, lines 19-23). *It should be noted that Shen does not expressly disclose a memory controller in the design. However, the citation noted above discloses reading from and writing to a cache memory. As one of ordinary skill in the art knows a memory controller is inherently required to interface with any memory.*

trend logic (col. 4, lines 40-43; Fig. 2, element 20);

wherein the processor executes instructions (col. 4, lines 36-37);

wherein the trend logic provides trend information about the stack to the controller (col. 5, lines 10-14 and 19-22; Fig. 2, elements 20, 24, 40, and 94); *It should noted that the trend information is calculated by the three-way addition of the stack pointer, segment base, and increment value (which comes from the increment logic) and then the trend information is sent from the three-port adder to the memory controller.*

wherein the trend information about the stack is based on at least one future instruction (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; Figs. 2 and 4).

16. **As per claim 13**, Shen discloses the trend logic determines a net stack trend based on current instruction and future instruction information coming from the decode logic (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15; col. 4, lines 36-60; Fig. 2, elements 20, 30, and 94).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claim 5 is rejected under 35 U.S.C. 103(a) as being obvious over Shen et al. in view of Ebrahim et al. (U.S. Patent 5,893,121).

19. Shen discloses all the limitations of claim 5 except the cache memory maintains a single dirty cache line for stack data.

Ebrahim discloses the cache memory maintains a single dirty cache line for stack data (col. 5, lines 32-35). *It should be noted that a cache block maintaining a dirty bit is analogous to a "dirty cache line".*

Shen and Ebrahim are analogous art because they are from the same field of endeavor, that being stack memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Ebrahim's stack cache memory containing a single dirty cache line within Shen's stack trend tracker system.

The motivation for doing so would have been to avoid writing back unmodified stack cache blocks to main memory (Ebrahim, col. 5, lines 33-35).

Therefore, it would have been obvious to combine Ebrahim with Shen for the benefit of obtaining the invention as specified in claim 5.

20. Claims 6 and 17-20 are rejected under 35 U.S.C. 103(a) as being obvious over Shen et al. in view of Steely et al. (U.S. Patent 6,801,986).

21. **As per claim 6**, Shen discloses all the limitations of claim 6 except determining which word of the dirty cache line is going to be written to.

Steely discloses determining which word of the dirty cache line is going to be written to (col. 2, lines 39-43). *It should be noted that when taking the broadest reasonable interpretation of the claim language it is clear that the limitations of the claim do not specify how many words are in a dirty cache line. Steely does not disclose the*

exact size of a cache line, however, at minimum it must contain one word, meaning a write request would always go to a predetermined word with a dirty cache line, that being the only word in the dirty cache line.

Shen and Steely are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Steely's dirty cache line write procedure with Shen's stack trend tracker system.

The motivation for doing so would have been to produce an atomic read/write sequence which reduces the number of system commands and so reduces system overhead during contention for a memory block by two or more processors in a multiprocessor computer system (Steely, col. 6, lines 14-18). *See col. 2, lines 46-49 for a definition of an "atomic read/write."*

Therefore, it would have been obvious to combine Steely with Shen for the benefit of obtaining the invention as specified in claim 6.

22. **As per claim 17**, Shen discloses a method, comprising:

determining whether the size of a stack is increasing or decreasing (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-7 and 9-10; Fig. 2).

Shen does not expressly disclose issuing a write request to a cache memory, wherein the cache memory includes multiple cache lines;

determining whether the write request refers to a predetermined word within a dirty cache line.

Steely discloses issuing a write request to a cache memory, wherein the cache memory includes multiple cache lines (col. 1, lines 51-52, col. 9, lines 61-62; Fig. 2A, element 221); *It should be noted that the presence of probe commands and cache tags indicate the cache memory has multiple cache lines.*

determining whether the write request refers to a predetermined word within a dirty cache line (Steely, col. 2, lines 39-43); *It should be noted that when taking the broadest reasonable interpretation of the claim language it is clear that the limitations of the claim do not specify how many words are in a dirty cache line. Steely does not disclose the exact size of a cache line, however, at minimum it must contain one word, meaning a write request would always go to a predetermined word with a dirty cache line, that being the only word in the dirty cache line.*

Shen and Steely are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Steely's dirty cache line write procedure with Shen's stack trend tracker system.

The motivation for doing so would have been to produce an atomic read/write sequence which reduces the number of system commands and so reduces system overhead during contention for a memory block by two or more processors in a multiprocessor computer system (Steely, col. 6, lines 14-18). *See col. 2, lines 46-49 for a definition of an "atomic read/write."*

Therefore, it would have been obvious to combine Steely with Shen for the benefit of obtaining the invention as specified in claim 17.

23. **As per claim 18**, the combination of Shen/Steely discloses determining whether the write request will be to the end of a dirty cache line (Steely, col. 8, lines 55-57; Fig. 2A, element 221). *It should be noted that when taking the broadest reasonable interpretation of the claim language it is clear that the limitations of the claim do not specify how many words are in a dirty cache line. Steely does not disclose the exact size of a cache line, however, at minimum it must contain one word, meaning a write request would always write bits to both the beginning and end of a dirty cache line.*

24. **As per claim 19**, the combination of Shen/Steely discloses the stack size is increasing (Shen, col. 5, lines 5-7) and the dirty cache line is written to a main memory (Steely, col. 9, lines 63-65; Fig. 1, elements 108 and 116; Fig. 2A, element 221).

25. **As per claim 20**, the combination of Shen/Steely discloses the stack size decreasing (Shen, col. 5, lines 9-10) and the dirty cache line is retained in the cache memory (col. 9, lines 63-67; Fig. 1, elements 108 and 116; Fig. 2A, element 221). *It should be noted that when taking the broadest reasonable interpretation of the claim language it is clear that the limitations of the claim do not specify how much time elapses before a dirty cache line is written back to main memory (i.e. how long the dirty cache is retained in cache memory). Steely discloses that the dirty cache line will be written back into main memory at some point in time.*

26. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being obvious over Shen et al. in view of O'Connor et al. (U.S. Patent 6,026,485).

27. **As per claim 12**, Shen discloses all the limitations of claim 12 except an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions.

O'Connor discloses an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions (col. 3, lines 5-10, 15-18, and 42-48). *It should be noted that first instructions are current instructions while second instructions are future instructions.*

Shen and O'Connor are analogous art because they are from the same field of endeavor, that being stack-based instruction processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use O'Connor's instruction decoder within Shen's stack trend tracker system.

The motivation for doing so would have been to identify foldable instruction sequences and supply an execution unit with an equivalent folded operation thereby reduce processing cycles otherwise required for decoding and executing multiple operations corresponding to the multiple instructions of the folded instruction sequence (O'Connor, col. 3, lines 20-25).

Therefore, it would have been obvious to combine O'Connor with Shen for the benefit of obtaining the invention as specified in claim 12.

28. **As per claim 14**, the combination of Shen/O'Connor discloses the second portion of the decoder is adjusted so that the number of future instructions that are decoded equals at least two (O'Connor, col. 3, lines 59-60). *It should be noted that first*

instructions are current instructions while second and third instructions are both future instructions.

Response to Arguments

29. Applicant's arguments, see page 19, the first full paragraph, of the communication filed May 15, 2006, with respect to the rejection **claim 18** under 35 USC § 102(b) have been fully considered and are persuasive. The rejection has been withdrawn. However, upon further consideration, new grounds of rejection have been made under 35 USC § 103 with respect to **claim 18** as presented above.

30. Applicant's arguments in the communication filed May 15, 2006 with respect to claims **1-17 and 19-20** have been fully considered but they are not persuasive.

31. Applicant argues in the first full paragraph of page 15 that "There is no teaching in Shen (col. 3, line 65, col. 7, line 7 and Fig. 2) for "examining" current and future instructions operating on a stack."

The Examiner respectfully disagrees and refers Applicant to Shen, col. 6, line 58 – col. 7, line 15 and Fig. 4 as cited above. Fig. 4 clearly shows that multiple instructions operating on the stack are being executed at the various stages of the pipelined processor. As with any pipelined processor, the various stages contain both current and future instructions. Also, when taking the broadest reasonable interpretation of the term "examining" it clear that the act of "executing" as disclosed by Shen requires the instructions to be "examined" at some instance in time before the execution may occur.

Accordingly, Shen's execution of stack instructions in the five-stage pipelined processor sufficiently teaches "examining current and future instructions operating on a stack."

32. Applicant argues in the second full paragraph of page 15 that "There is no teaching in Shen (col. 4, lines 11-15 and 36-60; and Fig. 2) for determining stack trend information."

The Examiner respectfully disagrees. Applicant has failed to give an explicit definition of what "trend information" specifically entails within the specification. Therefore, Applicant's allegation that a number (i.e. the stack pointer) is not a trend or trend information is incorrect. The stack pointer indicates the final value of the stack and therefore the stack pointer is an observation of how much the stack increments or decrements over a period of time. Thus, the stack pointer indicates a "trend" of how much the stack increments or decrements over a period of time. It is of no consequence that the stack pointer is a number. Numbers signify information. Accordingly, Shen's stack pointer sufficiently teaches "determining stack trend information."

33. Applicant argues in the second and third lines of page 16 that "Shen fails to teach or suggest..."trend logic."

The Examiner respectfully disagrees and refers Applicant to Shen, col. 4, lines 40-43; Fig. 2, element 20 as cited in the Office action dated November 23, 2005, which state "increment logic 20 determines increment value 94 to add to stack pointer 12..." As stated in paragraph 0023, lines 9-10 of Applicant's specification "For example, trend logic 21 may receive CURRENT 68 and FUTURE 70 to generate the trend information

about the stack 32." Thus, it is clear the increment logic determines the stack trend information (i.e. the stack pointer). Accordingly, Shen's increment logic sufficiently teaches "trend logic."

34. Applicant argues in the first full paragraph of page 16 that "Shen fails to teach or suggest, "utilizing the trend information to reduce data traffic between various levels of a memory.""

The Examiner respectfully disagrees and refers Applicant to rejection of claim 1 above in which the Examiner has added a new citation as well as a new citation note to more clearly describe Shen's teaching of "utilizing the trend information to reduce data traffic between various levels of a memory."

35. Applicant argues in the first full paragraph of page 16 that "Shen fails to teach or suggest..."wherein the trend information about the stack is based on at least one future instruction.""

The Examiner respectfully disagrees. As the stated directly above the various stages in Shen's pipelined processor contain both current and future instructions and Shen's stack pointer is equivalent to trend information. Accordingly, Shen sufficiently teaches "wherein the trend information about the stack is based on at least one future instruction."

36. Applicant argues in the last paragraph of page 24 that "There is no teaching in Shen (col. 3, line 65- col. 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-7 and 9-10; and Fig. 2) for "determining where the size of the stack is increasing or decreasing.""

The Examiner respectfully disagrees and refers Applicant above to section 31 of the current Office action.

37. Applicant argues in the first paragraph of page 27 that "Examiner fails to offer ANY rationale for combining Shen with Steely."

The Examiner respectfully disagrees and refers Applicant above to section 19 of the current Office action.

38. As for Applicant's arguments with respect to dependent claims 2-6, 8, 12-14, and 18-20, the arguments rely on the basis that independent claims 1, 11, and 17 are allowable and therefore for the same reasons dependent claims 2-6, 8, 12-14, and 19-20 are allowable. However, as described above in sections 29-35 of the current Office action independent claims 1, 11, and 17 are not patentably distinct over the cited prior, and therefore dependent claims 2-6, 8, 12-14, and 19-20 are also not patentably distinct over the cited prior for reasons described in the rejections above.

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

Allowable Subject Matter

39. **Claims 7, 9-10, and 15-16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

40. **Claims 7 and 9-10** also need to be rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 1st paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

41. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to disclose the combination including the limitations of:

(**Claims 7 and 15**) "...the trend information is used to restrict writing dirty cache lines from cache memory to main memory when the trend information indicates the stack size is decreasing."

(**Claim 9**) "...determining if a line is written back includes analyzing the trend information and includes examining a dirty cache line to determine which word of the dirty cache line is going to be written to."

(**Claim 16**) "...the dirty cache line is written to main memory if the trend information indicates the stack is increasing."

42. As allowable subject matter has been indicated, Applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

Claims Rejected in the Application

Per the instant office action, **claims 1-6, 8, 11-14, and 17-20** have received a second action on the merits and are subject of a second action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 6,990,567 (Cohen et al.) discloses use of internal general purpose registers of a processor as a Java virtual machine top of stack and dynamic allocation of the registers according to stack status.

2. U.S. Patent Application Publication 2003/0221035 (Adams) discloses a breakpoint handler may then be invoked to decrease the stack size whenever a pop operation occurs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
Art Unit 2185
August 18, 2006

SANJIV SHAH
PRIMARY EXAMINER